UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,386	08/01/2003	Gary Benjamin	200208210-1	2825

22879 7590 07/26/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
TERESINSKI, JOHN	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,386	BENJAMIN ET AL.	
	Examiner	Art Unit	
	John Teresinski	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-16,18-25 and 27-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-16,18-25 and 27-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 8-15, 19-24 and 28-31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,687,662 to McNamara et al..

Regarding claims 1, 12, 21 and 32, McNamara et al. disclose a system and method for automated design verification including receiving design information from a circuit design tool (column 3 lines 25-57), identifying an electrical circuit condition such as a noise event (column 5 lines 55-58), determining a design verification test (column 5 lines 15-35), evaluating the effectiveness of the design verification test in exercising the electrical circuit condition (column 5 lines 51-58) and determining a second design verification test and also evaluating the effectiveness of the second design verification test in exercising the electrical circuit condition when the first design verification test does not effectively exercise the electrical circuit condition (column 5 lines 51-63).

Regarding claims 2, 13 and 22, McNamara et al. disclose an exhaustive test definition process (column 5 lines 3-14).

Regarding claims 3, 14, 23 and 24, McNamara et al. disclose executing the design verification test in a simulator and recognizing the presence of the electrical circuit condition in the simulator results (column 3 lines 25-42).

Regarding claim 4, McNamara et al. disclose representing the electrical condition in a simulator monitor function, executing the design verification test and the simulator monitor function in a simulator, and monitoring the activity of the simulator monitor function (column 3 lines 37-42).

Regarding claims 8, 19 and 28, McNamara et al. disclose generating a description file readable by one or more of an automatic test pattern generator and causing an automatic test pattern to be executed using said generated description file as an input (column 3 lines 43-57).

Regarding claims 9 and 29, McNamara et al. disclose receiving the electrical circuit condition in a design verification tool and verifying the design of the electronic circuit based on the electrical circuit condition (column 5 lines 20-25).

Regarding claims 10, 11, 30 and 31, McNamara et al. disclose simulating a noise event and automatically generating a test pattern for testing a noise event (column 3 lines 25-57).

Regarding claims 15 and 20, McNamara et al. disclose directing the received electrical condition to a design verification tool, starting a design verification tool, receiving an output from the design verification tool, and issuing a signal when the identified electrical circuit condition is not detected in the received design verification tool output (column 3 lines 25-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 7, 16, 18, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over McNamara et al. in view of U.S. Patent No. 6,708,329 to Whitehill et al..

Regarding claims 5, 16 and 27, McNamara et al. disclose the system and method as described above including a lexical analyzer generating (column 6 lines 1-11). McNamara et al. does not disclose generating tokens or parsing an output report from a circuit design tool and generating tokens representing the parsed output report. Whitehill et al. disclose a method and apparatus for software conversion for translating simulation modes to software implementation including parsing an output report from a circuit design tool and generating tokens representing the data report (column 8 lines 35-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include parsing output to generate tokens as taught by Whitehill et al. into McNamara et al. for the purpose of narrowing the processing possibilities for a data line.

Regarding claims 7, 18 and 27, McNamara et al. disclose receiving data descriptive of the design information (column 6 lines 1-11). McNamara et al. does not disclose receiving tokens and analyze the structure of the tokens in accordance with a pre-established electrical event definition. Whitehall et al. disclose receiving tokens and analyze the structure of the tokens in

accordance with a pre-established electrical event definition (column 8 lines 50-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include receiving tokens and analyze the structure of the tokens as taught by Whitehall et al. into McNamara et al. for the purpose of providing a more detailed analysis of output data.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are cited to further show the state of the art with repesct to design verification methods and devices in general:

U.S. Patent No. 6,449,757 to Karniewicz discloses a semiconductor test structure design.

U.S. Patent No. 6,473,888 to Nassif et al. disclose a method and apparatus for calculating delays in a timing verifier circuit.

U.S. Patent No. 2004/0181763 o Soltis, JR. et al. disclose an automatic manufacturing test case generation method and system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Teresinski whose telephone number is (571) 272-2235. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JT

JT
July 26, 2005

EDWARD LEFKOWITZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800